Refine Search

Search Results -

Terms	Documents
L24 and (software ADJ testing) and (test adj case)	23

Database:

```
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins
```

Search:

```
L25
```

Refine Search

Recall Text   Clear   Interrupt

Search History

DATE: Sunday, September 10, 2006   **Purge Queries**   Printable Copy   Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=NO; OP=OR		
L25	L24 and (software ADJ testing) and (test adj case)	23	L25
L24	timer or timed or (event adj triggered) or event-triggered	193145	L24
L23	timer or timed or (event adj triggered) or event-trigger	193148	L23
L22	717/124-127,138.ccls. or 702/1,108.ccls. or 700/90,108,109.ccls. or 379/10.01.ccls. or 703/10,104.1.ccls. or 703/2,22,23.ccls.	4784	L22
L21	L19 ANd L15	1	L21
L20	L19 ANd L16	0	L20
L19	L18 ANd 717/$$$.ccls.	63	L19
L18	(Test ADJ case) and (Web OR Internet OR extrtanet OR intranet)	337	L18
L17	L15 AND L16	0	L17
L16	(6236952 5396170 5254942 6107815 5353240 4694242 5822615 4456994 3986106 4718112 4034195 6279124 5758061 6067639 6237138 5911041).pn.	16	L16

(6006022 6167401 6175812 6181615 6209110 6287765 6292830 6436703

L15	6766267 5745390 5954829 6157899 6381604 6387640 6395889 6421613 6442714 6477442 5394509 6381556 6430456 6683975 5519633 5546321 5699440 5774875 5778049 5787021 5838568 5854930 5949682 5995975 6032159 6090632 6115704 6125401 6134674 6192108 6230157 6338148 6536036 6620204 6695208 6741967 6742165 6754605 6801818 6823502 5716856 5857192).pn.	50	L15
L14	L13 AND (specific ADJ time)	24	L14
L13	Test ADJ plan	356	L13
L12	L10 AND ((GUI or (User ADJ interface)) same tester)	2	L12
L11	L10 AND ((GUI or (User ADJ interface)) AND tester).ab.	0	L11
L10	L9 AND (GUI or (User ADJ interface))	60	L10
L9	L8 AND L7	102	L9
L8	L6 AND (interval)	200	L8
L7	L6 AND (periodic)	149	L7
L6	L5 ANd (time or timer or batch)	748	L6
L5	(Software and testing) AND L4	761	L5
L4	(test ADJ case)	2250	L4
L3	(USe ADJ case)	0	L3
L2	(Software and testing) and (USe ADJ case)	0	L2
L1	(Software and testing and (USe ADJ case))	0	L1

END OF SEARCH HISTORY

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| software testing simulation case timer | | **Search** |

Scholar Results **11 - 20** of about **7,820** for **software testing simulation case timer** with **Safesearch on**. (0.1

Dummynet: a simple approach to the evaluation of network protocols All articles Recent articles - group of 12 »
L Rizzo - ACM SIGCOMM Computer Communication Review, 1997 - portal.acm.org
... of both **simulation** and real-world **testing**: great control ... or some other kind of
collaborative **software**, which want to ... small for the purposes of the **simulation**. ...
Cited by 421 - Related Articles - Web Search - BL Direct

Using **software** architecture for code **testing** - group of 7 »
H Muccini, A Bertolino, P Inverardi - IEEE Transactions on **Software** Engineering, 2004 -
doi.ieeecomputersociety.org
... also discusses the use of **software** architecture for ... takes into consideration
architecture testability, **simulation**, and slicing ... cycle of SA-based **testing** with ...
Cited by 23 - Related Articles - Web Search - BL Direct

Model Based **Testing** in Evolutionary **Software** Development - group of 20 »
A Pretschner, H Lotzbeyer, J Philipps - Proc. 11th IEEE Intl. Workshop on Rapid System Prototyping, 2001 -
doi.ieeecomputersociety.org
... understanding of the models, for **simulation** and code ... As **testing** requires some piece
of **software** that can ... Model based **testing** covers both test **case** derivation ...
Cited by 14 - Related Articles - Web Search

[BOOK] Hard Real-time Computing Systems: Predictable Scheduling Algorithms and Applications
GC Buttazzo - 2004 - Springer
Cited by 314 - Related Articles - Web Search - BL Direct

A Prototyping Language for Real-Time **Software** - group of 2 »
VB Luqi, V Berzins, RT Yeh - TSE, 1988 - doi.ieeecs.org
... of the prototype data is also a partial **simulation** of the ... IEEE TRANSACTIONS ON **SOFTWARE**
ENGINEERING. ... with a given tag (injec- tions), for **testing** whether a one ...
Cited by 66 - Related Articles - Web Search

Simics: A full system **simulation** platform - group of 6 »
PS Magnusson, M Christensson, J Eskilson, D ... - Computer, 2002 - ieeexplore.ieee.org
... Full system **simulation** supports the design, devel- opment, and **testing** of computer
hardware and **software** within a **simulation** framework that ...
Cited by 205 - Related Articles - Web Search - BL Direct

Using evolutionary **testing** to improve efficiency and quality in **software testing** - group of 2 »
H Sthamer, J Wegener, A Baresel - ... -Pacific Conference on **Software Testing** Analysis and Review, ..., 2002 -
systematic-**testing**.com
... and the nested structures in **software** systems, lead to ... Evolutionary **testing** enables
a fully automated search for ... available must be replicated in a **simulation**. ...
Cited by 9 - Related Articles - View as HTML - Web Search

Testing-a challenge to method and tool developers - group of 2 »
MA Ould - **Software** Engineering Journal, 1991 - ieeexplore.ieee.org
... conditions and events that the **software** is required ... detect' Host and target environment
testing are well ... The main difficulty will be the thorough **simulation**. ...
Cited by 19 - Related Articles - Web Search

Testing Concurrent Reactive Systems with Constraint Logic Programming - group of 12 »
H Lotzbeyer, A Pretschner - Proc. 2nd workshop on Rule-Based Constraint Reasoning and ..., 2000 - in.tum.de
... 5 **Testing** ... approach to test **case** generation fits into this terminology, and explain
why **simulation** can be viewed as a special **case** of test **case** generation. ...
Cited by 14 - Related Articles - View as HTML - Web Search

Software Performance Engineering: A **Case** Study Including Performance Comparison - group
of 6 »
CU Smith - IEEE TRANSACTIONS ON **SOFTWARE** ENGINEERING, 1993 - doi.ieeecomputersociety.org
... in the winter and summer **simulation** conferences ... draw an analogy between modeling
and **testing**, both of ... the **case** study design and **Software** Performance Engineering ...
Cited by 58 - Related Articles - Web Search - BL Direct

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Result Page: **Previous** 1 **2** 3 4 5 6 7 8 9 1011   **Next**

| software testing simulation case time | Search |

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Set	Items	Description
S1	27	TESTCASE? OR CASE? ?(2N)(TEST OR TESTS OR TESTED OR TESTING)
S2	121	SIMULAT?R? ?
S3	231	BATCH? OR BATCHQUEUE?
S4	16	TESTDRIVE? OR TEST()DRIVE? ?
S5	106	QUEUE? ?
S6	27096	SOFTWARE? OR SOFT()WARE? ? OR APPLICATION? ? OR APP? ?
S7	871	S6(3N)(TEST OR TESTS OR TESTED OR TESTING OR TRIAL? ?)
S8	5498	TRIGGER? OR SPECIFIC OR SPECIFIED OR DESIGNATED OR SCHEDUL? OR APPOINT??? OR PARTICULAR OR DEFINED OR DEFINITE OR STATED OR SELECTED
S9	5404	DETERMINED OR DENOTED OR TARGETED OR CERTAIN OR CHOSEN OR IDENTIFIED OR STIPULATED OR PRESCRIBED OR DECIDED OR SET OR GIVEN
S10	944	ESTABLISHED OR ARRANGED OR PREDESIGNATED OR PRESCHEDULED OR PREAPPOINTED OR PREDEFINED OR PRESTATED OR PRESELECTED OR PREDETERMINED
S11	92	PRETARGETED OR PRECHOSEN OR PREIDENTIFIED OR PRESTIPULATED OR PREDECIDED OR PRESET OR PREESTABLISHED OR PREARRANGED OR PRESPECIFIED
S12	102	PREPROGRAM? OR PRE()PROGRAM???? OR PRECONFIGURED OR PRE()CONFIGURED
S13	456	FIXED
S14	212	S8:S13(2W)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TIMELINE?)
S15	65	TIMED OR TIME()DEPENDENT OR TIMEDEPENDENT OR (TIMING OR TIME)(1W)CIRCUIT? OR TIMER? ?
S16	11	S14:S15(7N)(EXECUTE? ? OR EXECUTION OR EXECUTING OR RUN OR RUNS OR RAN OR RUNNING)
S17	11	S14:S15(7N)(EXERCIS? OR PERFORM? OR DEPLOY? OR LAUNCH? OR ACTIVAT? OR ACTUAT? OR EVOK? OR EVOC? OR INVOK? OR INVOC? OR ENABL? OR INABL?)
S18	14	S14:S15(7N)(INITIALIS? OR INITIALIZ? OR IMPLEMENT? OR START??? OR BEGIN? ? OR BEGAN OR BEGUN OR COMMENC????? OR CALL? ? OR CALLED OR CALLING)
S19	8	S14:S15(7N)(PROCESS OR PROCESSED OR PROCESSING OR PROCESSES OR HANDL???)
S20	6	(S1:S5 OR S7 OR SIMULATION?) AND S16:S19
S21	0	TIMETRIGGER?
S22	6	TRIGGER?(3N)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TIMELINE?)
S23	2	TRIGGER?(3N)(TIMED OR TIMEDEPENDENT OR TIMING OR TIMER? ?)
S24	0	(S1:S5 OR S7 OR SIMULATION?) AND S22:S23

20/7/5
DIALOG(R)File 256:TecInfoSource
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00139131   DOCUMENT TYPE: Review

PRODUCT NAMES: NetEnforcer 201 & 301 (019607); PacketShaper 2500 & 8500
(671096); QoSWorks 10000 (791768)

TITLE: Searching for the QoS Holy Grail: Implementing QoS in enterprise...
AUTHOR: Griffin, Chris; Goddard, Greg
SOURCE: Network World,   v19 n22 p53(5) Jun 3, 2002
ISSN: 0887-7661
HOMEPAGE: http://www.nwfusion.com

FILE SEGMENT: Review
RECORD TYPE: Product Analysis
GRADE: Product Analysis, No Rating

Allot Communications' NetEnforcer, Packeteer's PacketShaper 2500 & 8500,
and Sitara Networks' QoSWorks 10000 are among enterprise network QoS
(quality of service) implementations tested. QoS is a multifarious
gathering of technologies and methods that when effectively chosen and
implemented can ensure that real-time and business traffic have available
the bandwidth they need when traversing a LAN. Stages of QoS include
classification; marking with such tags as 802.1p, Differentiated Services
Code Point, or IP Precedence; and enforcement, which uses both information
learned in the classification stage and current network conditions to
establish how packets should be handled at a given   time . QoS
equipment from five vendors was tested on a simulated frame relay network.
Test scenarios included an outbound denial of service attack. NetEnforcer
201 and 301, two LAN-based appliances, accept IP Precedence and DSCP-tagged
traffic. They are most appropriate for companies that need high levels of
flexibility and customization abilities. PacketShaper 2500 and 8500 have
excellent performance with an intuitive GUI, while LAN expansion modules
are available for each PacketShaper model and allow multiple networks to be
controlled from the same appliance. They are most appropriate for high
bit-rate connections and networks that are close together to minimize the
number of appliances. QoSWorks 10000 has good performance, queue depth
controls, and is recommended for low latency traffic situations.

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        (c) 1999 PR Newswire Association Inc
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        (c) 2006 PR Newswire Association Inc
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        (c) 1999 Business Wire
File 610:Business Wire 1999-2006/Sep 12
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        (c) 1999 The Gale Group
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        (c) 2006 The Gale Group
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        (c) 2006 McGraw-Hill Co. Inc
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        (c) 2006 The Gale Group
File 647:CMP Computer Fulltext 1988-2006/Oct W4
        (c) 2006 CMP Media, LLC
File 674:Computer News Fulltext 1989-2006/Sep W1
        (c) 2006 IDG Communications

Set	Items	Description
S1	39470	TESTCASE? OR CASE? ?(2N)(TEST OR TESTS OR TESTED OR TESTIN-G)
S2	496483	SIMULAT?R? ? OR SIMULATION? ?
S3	267060	BATCH? OR BATCHQUEUE?
S4	49443	TESTDRIVE? OR TEST()DRIVE? ?
S5	131441	QUEUE? OR QUEU???
S6	13488761	SOFTWARE? OR SOFT()WARE? ? OR APPLICATION? ? OR APP? ?
S7	291031	S6(3N)(TEST OR TESTS OR TESTED OR TESTING OR TRIAL? ?)
S8	15181170	SPECIFIC OR SPECIFIED OR DESIGNATED OR SCHEDUL? OR APPOINT-??? OR PARTICULAR OR DEFINED OR DEFINITE OR STATED OR SELECTED
S9	16326539	DETERMINED OR DENOTED OR TARGETED OR CERTAIN OR CHOSEN OR -IDENTIFIED OR STIPULATED OR PRESCRIBED OR DECIDED OR SET OR G-IVEN
S10	3660482	ESTABLISHED OR ARRANGED OR PREDESIGNATED OR PRESCHEDULED OR PREAPPOINTED OR PREDEFINED OR PRESTATED OR PRESELECTED OR PR-EDETERMINED
S11	57412	PRETARGETED OR PRECHOSEN OR PREIDENTIFIED OR PRESTIPULATED OR PREDECIDED OR PRESET OR PREESTABLISHED OR PREARRANGED OR P-RESPECIFIED
S12	75663	PREPROGRAM? OR PRE()PROGRAM???? OR PRECONFIGURED OR PRE()C-ONFIGURED
S13	1677894	FIXED
S14	553624	S8:S13(2W)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TI-MELINE?)
S15	195302	TIMED OR TIME()DEPENDENT OR TIMEDEPENDENT OR (TIMING OR TI-

```
                    ME)(1W)CIRCUIT? OR TIMER? ?
S16      12541    S14:S15(7N)(EXECUTE? ? OR EXECUTION OR EXECUTING OR RUN OR
                    RUNS OR RAN OR RUNNING)
S17      26957    S14:S15(7N)(EXERCIS? OR PERFORM? OR DEPLOY? OR LAUNCH? OR -
                    ACTIVAT? OR ACTUAT? OR EVOK? OR EVOC? OR INVOK? OR INVOC? OR -
                    ENABL? OR INABL?)
S18      76324    S14:S15(7N)(INITIALIS? OR INITIALIZ? OR IMPLEMENT? OR STAR-
                    T??? OR BEGIN? ? OR BEGAN OR BEGUN OR COMMENC????? OR CALL? ?
                    OR CALLED OR CALLING)
S19      15089    S14:S15(7N)(PROCESS OR PROCESSED OR PROCESSING OR PROCESSES
                    OR HANDL???)
S20         30    TIMETRIGGER?
S21       9065    TRIGGER?(3N)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? -
                    OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR
                    TIMELINE?)
S22       1525    TRIGGER?(3N)(TIMED OR TIMEDEPENDENT OR TIMING OR TIMER? ?)
S23       2854    (S1:S5 OR S7)(S)S16:S22
S24       1169    S23(S)S6
S25         61    S1(S)S16:S22
S26        405    S7(S)S16:S22
S27          5    S26(S)S1
S28         85    S26(S)S16
S29    2571399    S6(5N)DEVELOP????
S30         54    S26(S)S29
S31        193    S25 OR S27:S28 OR S30
S32         64    S31/2001:2006
S33        129    S31 NOT S32
S34         90    RD  (unique items)
```

 34/3,K/2   (Item 2 from file: 9)
DIALOG(R)File   9:Business & Industry(R)
(c) 2006 The Gale Group. All rts. reserv.

01090101 Supplier Number: 23684479
WebQualify Puts Systems Through Their Paces
(Radview Software Inc introducing WebQualify for stress-testing intranets)
Interactive Week, v 3, n 23, p 56
October 28, 1996
DOCUMENT TYPE: Journal ISSN: 1078-7259 (United States)
LANGUAGE: English RECORD TYPE: Abstract

ABSTRACT:
Radview Software Inc (Israel) is introducing WebQualify, a **software**
package for stress **testing** intranets. The program is divided into two
components, WebLoad and Internet Test. WebLoad executes and monitors load
stress **tests** and determines Web **application** performance under
user-defined system loads. Tests may be generated remotely on multiple
client workstations, either real or simulated. WebLoad **executes** user- and
system-defined **timers** for participating clients indicating when a
request was sent, received, transmitted and completed. This data...

 34/3,K/6   (Item 3 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2006 ProQuest Info&Learning. All rts. reserv.

01917197 05-68189
Engineers embrace CompactPCI
Bassak, Gil
Test & Measurement World v19n13 PP: 12-16 Oct 15, 1999
ISSN: 0744-1657 JRNL CODE: CTMW

...ABSTRACT: range of CompactPCI instrument cards, engineers can make use
of an abundance of PC-compatible **application** **software** and **development**
tools. **Test** and measurement engineers also can get the added features of

CompactPCI's 2-year-old PCI extensions for Instrumentation (PXI). This
superset of CompactPCI adds **timing** and **triggering** functions, imposes
requirements for documenting environmental tests, and establishes a
standard Windows-based software framework...

34/3,K/10   (Item 7 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
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01403880 00054867
Code cracker
Feibus, Andy
Informationweek n620 PP: 1A-4A Mar 3, 1997
ISSN: 8750-6874 JRNL CODE: IWK
WORD COUNT: 1608

...TEXT: case that will verify the contents of the form's customer name
field.

SQA supports **test** **cases** to compare not only alphanumeric objects but
also menus, lists, data-bound OCX/ActiveX controls (such as grids) and
nonvisual objects. Users can also define **test** **cases** to compare object
properties, file existence, and window existence. If you are interested in
determining an application's performance during part of the test procedure,
you can also define **start** and stop points for a test **timer** . These **test**
  cases help validate your project at whatever programming level you need
to be sure the application...

34/3,K/12   (Item 9 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
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01235593 98-84988
The mysteries of load testing
Straathof, Jeff
UNIX Review v14n8 PP: 33-40 Jul 1996
ISSN: 0742-3136 JRNL CODE: UXR
WORD COUNT: 3069

...TEXT: logical transactions that include database communication. Or, a
recording tool will let you interactively specify **timers** during
execution . If you forget to do it at capture time, you simply can add
timers to...

...tests should use at least one pacing function to control the load placed
on the **application** under **test** . You should not use thinking and typing
time alone to adjust the load. Only pacing functions let you control the
load accurately because a slowdown of the **application** under **test** and
subsequent increases in response times would lighten the load imposed by
the driver if...

34/3,K/15   (Item 12 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
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00654050 93-03271
Bank Uses OS/2 to Monitor Mainframe
Van Brussel, Carolyn
Computing Canada v18n24 PP: 30 Nov 23, 1992
ISSN: 0319-0161 JRNL CODE: CCD

...ABSTRACT: in conjunction with the company's Strobe Application

Performance Measurement System. Strobe produces profiles of running
applications within specified periods of time . The reports help to
locate problems and determine hardware and software resource allocation.
Programart typically...

...Royal Bank of Canada is a beta site for the APMPower tool, using it to
test new **applications** before they are implemented.

 34/3,K/22   (Item 2 from file: 610)
DIALOG(R)File 610:Business Wire
(c) 2006 Business Wire. All rts. reserv.

00312564 20000630182B4124 (USE FORMAT 7 FOR FULLTEXT)
Telelogic Tau Logiscope 5.0 Ensures Best Practices for C/C++/Java/Ada
Applications
Business Wire
Friday, June 30, 2000 05:36 EDT
JOURNAL CODE: BW LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
DOCUMENT TYPE: NEWSWIRE
WORD COUNT: 767

...test scripting language TTCN, in the Telelogic Tau TTCN Suite. These
tools
provide a complete **software** **development** , simulation and **testing**
environment
for real-time and communications applications. Telelogic Tau also offers
SCADE
(Safety Critital **Application** **Development** Environment), a tool for
developing
 time - **triggered** , safety-critical systems and Logiscope, a tool suite
that
facilitates quality assessments of software written...
? t34/3,k/35,40,42,47,51,56,63

 34/3,K/35   (Item 4 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
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04141530   SUPPLIER NUMBER: 16252526   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Testing your data depository with NetBench 3.0. (Ziff-Davis Benchmark
   Operation benchmarking utility) (includes related articles on how to get
   a copy of NetBench, highlights) (PC Tech: Lab Notes)(Column) (Tutorial)
Catchings, Bill; Van Name, Mark L.
PC Magazine, v13, n17, p340(3)
Oct 11, 1994
DOCUMENT TYPE: Tutorial   ISSN: 0888-8507   LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2413   LINE COUNT: 00184

...   test a huge number of products, so NetBench has strong support for
automated and customized **testing** . The controller **software** lets you
create **test** mixes that run exactly the tests you designate with the
parameters of your choice. For each mix, you can specify how long the tests
will **run** before the **timer** starts and after it stops--quantities known
as ramp-up and ramp-down time. (A server...

 34/3,K/40   (Item 9 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
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03694162   SUPPLIER NUMBER: 11674986   (USE FORMAT 7 OR 9 FOR FULL TEXT)
WinTools 1.0 furnishes potent desktop builder. (Software Review) (First
   Look) (Evaluation)

Sullivan, Eamonn
PC Week, v9, n1, p29(2)
Jan 6, 1992
DOCUMENT TYPE: Evaluation   ISSN: 0740-1604   LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 639   LINE COUNT: 00049

...   in WinTools is based on its Tools. Each tool can be set to open and
run at **scheduled   times** , and special tools can be used to send DDE
messages or keystroke macros to other Windows **applications** . In **tests** ,
one icon, for instance, controlled Word to remove line endings from text
downloaded from the...

    34/3,K/42   (Item 11 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
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03021523   SUPPLIER NUMBER: 06109426   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Ethernet Analyzer. (Excelan Inc.) (Hardware Review) (one of four products
    evaluated in 'Making connections: LAN analyzers')** (evaluation)
Derfler, Frank J., Jr.; Campbell, Greg
PC Magazine, v6, n22, p252(3)
Dec 22, 1987
DOCUMENT TYPE: evaluation   ISSN: 0888-8507   LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1586   LINE COUNT: 00121

...   have set all the filters, triggers, and other options, the settings
are saved as a **test** file. The Lanz **software** can then run **tests** by
using these files to configure the triggering, monitoring, filtering, data
capture, and traffic generation functions. Tests can **run** automatically at
a **specified   time** , they can be programmed to **run** when a specific
network event is detected, or they can be run manually.
    The software...

    34/3,K/47   (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

09344757   SUPPLIER NUMBER: 19178347   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Code cracker. (SQA's SQA Suite TeamTest Edition 5.1 automatic code-testing
    software) (Software Review)(Evaluation)**
Feibus, Andy
InformationWeek, n620, p1A(3)
March 3, 1997
DOCUMENT TYPE: Evaluation   ISSN: 8750-6874   LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1750   LINE COUNT: 00138

...   determining an application's performance during part of the test
procedure, you can also define **start** and stop points for a test **timer** .
These **test   cases** help validate your project at whatever programming
level you need to be sure the application...

    34/3,K/51   (Item 7 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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08272726   SUPPLIER NUMBER: 17610814   (USE FORMAT 7 OR 9 FOR FULL TEXT)
**Peace of Mind for all but Power Mac users. (DigiSoft Inc's Peace of Mind
    3.0.2 utility software) (Software Review)(Evaluation)**
Ramsey, David

MacWEEK, v9, n45, p58(1)
Nov 13, 1995
DOCUMENT TYPE: Evaluation   ISSN: 0892-8118   LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1328   LINE COUNT: 00106

...   memory bit is affected by adjacent bits. You can set any group of
tests to run continuously for a specified period of time -- a handy
feature if your system has intermittent problems.
      The SCSI tests simulate worst-case...

 34/3,K/56   (Item 12 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

06166162   SUPPLIER NUMBER: 12804123   (USE FORMAT 7 OR 9 FOR FULL TEXT)
ITC '92 integrates design and test. (International Test Conference mixes
   state-of-the art technology and practical applications advice)
Novellino, John
Electronic Design, v40, n19, p65(3)
Sept 17, 1992
ISSN: 0013-4872   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1560   LINE COUNT: 00125

...   hungry for practical 'how-to' information on a wide variety of test
topics, including design/ test integration, software testing , and
test synthesis. This year's technical program combines papers, tutorials,
and panels to address these topics...

...time needed for testing. In the paper "Scan-Parity Design to Reduce the
Cost of Test Applications " (15.1), the authors propose a way to combine
scan design and parity testing to...

...using boundary-scan testing in a chip design and the ensuing savings.
      PAPERS DISCUSS SELF- TEST
      BIST applications are also well represented. Two papers address
concerns about the hardware overhead needed to implement...

...of "Self-Test Scheduling with Bounded Test Execution Time" (5.3)
describe test schedules that execute within a user- specified   time
limit, yet obtain high fault coverage with minimal hardware. Self-checking,
Concurrent Testing, and Self...

 34/3,K/63   (Item 19 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

03502229   SUPPLIER NUMBER: 06592015   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Space-age printer. (laser printer used for insurance forms)
Schultz, Beatta
Best's Review - Life-Health Insurance Edition, v88, n12, p111(2)
April, 1988
ISSN: 0005-9706   LANGUAGE: ENGLISH   RECORD TYPE: FULLTEXT
WORD COUNT: 2244   LINE COUNT: 00188

...   to preset the PC to begin processing at a specified time and begin
playback of test   cases . Version 5.0 also offers a security enhancement
that protects the play control files from...
? t34/3,k/82,90

 34/3,K/82   (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2006 The Gale Group. All rts. reserv.

01062051   Supplier Number: 40269172 (USE FORMAT 7 FOR FULLTEXT)
Travelers subsidiary releases new version of personal-computer-based
  testing product.
News Release, pN/A
Jan 18, 1988
Language: English   Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 471

...   automatic
    start-up feature enables users to preset the PC to "wake up" at a
    specified   time and begin playback of test   cases .

    The security enhancement protects the play control files from
    unintentional disruption by locking the Escape...

 34/3,K/90   (Item 2 from file: 674)
DIALOG(R)File 674:Computer News Fulltext
(c) 2006 IDG Communications. All rts. reserv.

 043612
The virtual watercooler
NetworkWorld TEST ALLIANCE
A new breed of group conferencing software lets employees chat without
    leaving their desks.
Byline: Steven Goldberg
Journal: Network World   Page Number: 57
Publication Date: April 10, 1995
Word Count: 3388   Line Count: 322

Text:
... conference, and it provides excellent browsing, searching and sorting
functionality. The one constant among our test bed of applications is
exclusive client support for Windows. On the server side, the product
requirements range from...

... in the appropriate level of the category hierarchy. For example,
consider a forum about the development of a new piece of software . Any
user with the appropriate privileges could create categories for marketing
and engineering. Within the... here is that these indices reside on the
OpenMind server. Index updates can occur at scheduled times , or they
can be set to run constantly in the background. This is a clear benefit
of OpenMind's client/server architecture...

```
File 348:EUROPEAN PATENTS 1978-2006/ 200636
        (c) 2006 European Patent Office
File 349:PCT FULLTEXT 1979-2006/UB=20060907UT=20060831
        (c) 2006 WIPO/Thomson
File 350:Derwent WPIX 1963-2006/UD=200657
        (c) 2006 The Thomson Corporation
```

Set	Items	Description
S1	12595	TESTCASE? OR CASE? ?(2N)(TEST OR TESTS OR TESTED OR TESTIN-G)
S2	94360	SIMULAT?R? ? OR SIMULATION? ?
S3	163105	BATCH? OR BATCHQUEUE?
S4	908	TESTDRIVE? OR TEST()DRIVE? ?
S5	58363	QUEUE? OR QUEU???
S6	3514168	SOFTWARE? OR SOFT()WARE? ? OR APPLICATION? ? OR APP? ?
S7	37291	S6(3N)(TEST OR TESTS OR TESTED OR TESTING OR TRIAL? ?)
S8	4200599	SPECIFIC OR SPECIFIED OR DESIGNATED OR SCHEDUL? OR APPOINT-??? OR PARTICULAR OR DEFINED OR DEFINITE OR STATED OR SELECTED
S9	3932669	DETERMINED OR DENOTED OR TARGETED OR CERTAIN OR CHOSEN OR -IDENTIFIED OR STIPULATED OR PRESCRIBED OR DECIDED OR SET OR G-IVEN
S10	3168535	ESTABLISHED OR ARRANGED OR PREDESIGNATED OR PRESCHEDULED OR PREAPPOINTED OR PREDEFINED OR PRESTATED OR PRESELECTED OR PR-EDETERMINED
S11	309440	PRETARGETED OR PRECHOSEN OR PREIDENTIFIED OR PRESTIPULATED OR PREDECIDED OR PRESET OR PREESTABLISHED OR PREARRANGED OR P-RESPECIFIED
S12	30520	PREPROGRAM? OR PRE()PROGRAM???? OR PRECONFIGURED OR PRE()C-ONFIGURED
S13	1650075	FIXED
S14	477747	S8:S13(2W)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TI-MELINE?)
S15	204011	TIMED OR TIME()DEPENDENT OR TIMEDEPENDENT OR (TIMING OR TI-ME)(1W)CIRCUIT? OR TIMER? ?
S16	18937	S14:S15(7N)(EXECUTE? ? OR EXECUTION OR EXECUTING OR RUN OR RUNS OR RAN OR RUNNING)
S17	59468	S14:S15(7N)(EXERCIS? OR PERFORM? OR DEPLOY? OR LAUNCH? OR -ACTIVAT? OR ACTUAT? OR EVOK? OR EVOC? OR INVOK? OR INVOC? OR -ENABL? OR INABL?)
S18	59932	S14:S15(7N)(INITIALIS? OR INITIALIZ? OR IMPLEMENT? OR STAR-T??? OR BEGIN? ? OR BEGAN OR BEGUN OR COMMENC????? OR CALL? ? OR CALLED OR CALLING)
S19	38440	S14:S15(7N)(PROCESS OR PROCESSED OR PROCESSING OR PROCESSES OR HANDL???)
S20	18	TIMETRIGGER?
S21	12023	TRIGGER?(3N)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? -OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TIMELINE?)
S22	6314	TRIGGER?(3N)(TIMED OR TIMEDEPENDENT OR TIMING OR TIMER? ?)
S23	2802	(S1:S5 OR S7)(25N)S16:S22
S24	92	S23(25N)S7
S25	46	S23(25N)S1
S26	48686	S6(5N)DEVELOP????
S27	20	S23(25N)S26
S28	46	S1(25N)S16:S22
S29	4	S28(25N)(SOFTWARE OR SOFT()WARE? ?)
S30	65	S25 OR S27:S29
S31	38	S30 AND AC=US/PR AND AY=(1963:2001)/PR
S32	39	S30 AND AC=US AND AY=1963:2001
S33	39	S30 AND AC=US AND AY=(1963:2001)/PR
S34	46	S30 AND PY=1963:2001
S35	51	S31:S34

?

? t35/5,k/44

00145630
TEST AUTOMATION SYSTEM
SYSTEME D'AUTOMATISATION D'ESSAIS
Patent Applicant/Assignee:
  AMERICAN TELEPHONE & TELEGRAPH COMPANY,
Inventor(s):
  ARCHIE Kent Clayton,
  FONOROW Owen Richard,
  MCGOULD Mary Catherine,
  MCLEAR Robert Ernst III,
  READ Edward Cameron,
  SCHAEFER Edwin Martin III,
  SCHWAB Suzanne Elvera,
  WODARZ Dennis,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 8802515 A1 19880407
  Application: WO 87US1570 19870625 (PCT/WO US8701570)
  Priority Application: US 86799 19860929
Designated States:
(Protection type is "patent" unless otherwise stated - for applications
prior to 2004)
  AT BE CH DE FR GB IT JP KR LU NL SE
Main International Patent Class (v7): G06F-015/20
International Patent Class (v7): G06F-11:26
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 13957

English Abstract
   A test automation system (Fig. 1) comprises storage and process
components connected by file interfaces. BPLAN (103) creates and stores
test descriptions in test information database (102). Tests are stored in
test storage hierarchy (100). BSYNC (104) completes test descriptions in
database (102) form contents of hierarchy (100). BQUERY (105) examines
descriptions and selects tests for execution. TESTLOCS file (106)
identifies selected tests. BQUERY (105) uses BBC (118) to communicate
requests for tests and test descriptions to other systems. BBCMON (120)
causes BQUERY (105) to satisfy requests and uses BBC (118) to communicate
responses to requesting systems. BDLOAD (107) gathers tests identified by
file (106) from hierarchy (100) into file (117) for downloading from host
(10) to target (11) processor. BRUN (109) executes downloaded tests,
collects test results in files (110-112), and reports result summaries.
BULOAD (113) assembles files (110-112) into file (114) for uploading to
processor (10). BSTORE (115) stores uploaded results in results database
(116). BQUERY (105) examines test results collected in database (116).

French Abstract
   Un systeme d'automatisation d'essais (Fig. 1) comprend des composants de
stockage et de traitement connectes par des interfaces de fichiers. BPNAN
(103) cree et stocke des descriptions d'essais dans une base de donnees
(102) d'informations d'essais. Les essais sont memorises dans une
hierarchie (100) de memorisation d'essais. BSYNC (104) acheve les
descriptions d'essais dans la base de donnees (102) a partir du contenu
de la hierarchie (100). BQUERY (105) examine les descriptions et
selectionne les essais en vue de leur execution. Le fichier TESTLOCS
(106) identifie les essais selectionnes. BQUERY (105) utilise BBC (118)
pour transmettre a d'autres systemes les demandes d'essais et de

descriptions d'essais. BBCMON (120) oblige BQUERY (105) a satisfaire ces
demandes et fait appel a BBC (118) pour communiquer les reponses aux
systemes demandeurs. BDLOAD (107) regroupe dans le fichier (117) a partir
de la hierarchie (100) les essais identifies par le fichier (106), en vue
de leur transfert depuis le processeur central (10) vers le processeur
destinataire (11). BRUN (109) execute les essais transferes, rassemble
les resultats d'essais dans les fichiers (110-112), et sort des etats
recapitulatifs des resultats. BULOAD (113) regroupe les fichiers
(110-112) en un fichier (114) pour telechargement vers le processeur
(10). BSTORE (115) stocke dans la base de donnees de resultats (116) les
resultats telecharges. BQUERY (105) examine les resultats d'essais
rassembles dans la base de donnees (116).

Patent and Priority Information (Country, Number, Date):
  Patent: ... 19880407
Fulltext Availability:
  Detailed Description
Publication Year: 1988

Detailed Description
... SETUP and PROCEDURE are specified by STIME
  field 313 and PTIME field 312r respectivelyr of test
   case file 300F while the time limit on CLEANUP is
predetermined for the system. When process 109
begins script execution , it also commences timing of
the specified time limitr at
steps 1012, 1014, and 1016. If at steps 1013p 1015,
or 1017, the...
? t35/69,k/49-51
>>>Format 69 is not valid in file 348

 35/69,K/49   (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corporation. All rts. reserv.

0008788240 - Drawing available
WPI ACC NO: 1998-332640/
XRPX Acc No: N1998-259658
Stress testing managing method using computer for telecommunication system
- involves selecting bulk call generator from available list and
designating mix of call programs of group to be run on it
Patent Assignee: MCI COMMUNICATIONS CORP (MCIC-N)
Inventor: BADGER B S; NEWMAN C E; WILLIAMS E E
Patent Family (1 patents, 1 countries)
Patent   Application
Number   Kind Date   Number   Kind   Date   Update
US 5761272   A   19980602 US 1996753550 A   19961126 199829 B

Priority Applications (no., kind, date): US 1996753550 A 19961126

Patent Details
Number   Kind Lan Pg Dwg Filing Notes
US 5761272   A   EN   16   10

  Alerting Abstract US A
  The method involves displaying a list of available originating bulk call
generators (17a-17n) and list of terminating bulk call generators
(19a-19n). Then, a particular bulk call generator is selected by user.
  Then, a group is formed by associating test case scripts with call
programs. Then, a mix of call programs of group to be run on selector bulk
call generators is designated.
  ADVANTAGE - Provides convenient user friendly call. Performs stress
testing without programming bulk call generator.

Title Terms/Index Terms/Additional Words: STRESS; TEST; MANAGE; METHOD;

COMPUTER; TELECOMMUNICATION; SYSTEM; SELECT; BULK; CALL; GENERATOR;
AVAILABLE; LIST; DESIGNATED; MIX; PROGRAM; GROUP; RUN

Class Codes
International Classification (Main): H04M-001/00
 (Additional/Secondary): H04M-003/08

File Segment: EPI;
DWPI Class: W01
Manual Codes (EPI/S-X): W01-A06A; W01-A06B5A; W01-A06E2A; W01-C02A1A

Original Publication Data by Authority

Original Abstracts:
...selected bulk call generators through the interface. The system also
displays a list of available **test** case scripts. The system enables the
user to formulate a mix of scripts to be executed by displaying a control
for each selected **test** **case** script. The system further enables a user
to designate different mixes of scripts for **selected** **time** periods over
a test **run** . The system then assigns each script to a call program and a
group of call...
Claims:
...23. /b A method of managing telecommunications testing, which comprises
the computer implemented steps of:associating **test** **case** scripts with
call programs to form a set; and,designating different mixes of call
programs of said set to be **run** on selected bulk **call** generators for
selected **time** periods over a stress test **run**.

 35/69,K/50   (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008001442 - Drawing available
WPI ACC NO: 1997-093659/
XRPX ACC NO: N1997-077538
**Open system interconnection test system used for executing compatibility
test between products manufactured to OSI standard - has higher order
tester to perform control and observation of service primitive of
installation of test and lower order tester to monitor actual transmission
and reception**
Patent Assignee: KODO TSUSHIN SYSTEM KENKYUSHO KK (KODO-N)
Inventor: HATAFUKU M
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
JP 8331203	A	19961213	JP 1995133200	A	19950531	199709	B

Priority Applications (no., kind, date): JP 1995133200 A 19950531

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
JP 8331203	A	JA	7	4	

  Alerting Abstract JP A
  The open system interconnection test system (10) receives the protocol
installation compatibility description document of the installation for a
test. A static test is performed by appropriate module to automatically
judged logical compatibility and interactive connectability. A higher order
tester (21) is provided at the higher level of the test installation. A
performed type sub- **test** **case** is loaded from the test system. Based on
the indication from the test system, the sub- **test** **case** is referred at
the **designated** **time** . The described test is **performed** by appropriate
device. The higher order tester processes the result of the described test.
In a lower order tester (14) the data actually transmitted and received
between the lower order tester and the higher order tester is controlled

and monitored.

For this purpose, communication unity is provided between the lower order tester and the higher order tester through a test manager (11). The data is exchanged between the higher and lower order tester is analysed according to the performed time sub-test case. Next, the test is repeated by executing operation such as substitution, delay using the lower order tester. An abnormality test is then performed. A comprehensive test result is judged from a sub-judgment of a higher order and a lower order tester. The output of the test result is formatted according to predetermined layout. While finalising the test, the dynamic test is performed and a test report is generated automatically.

ADVANTAGE - Reduces connection test time. Performs compatibility and interconnection test automatically.

Title Terms/Index Terms/Additional Words: OPEN; SYSTEM; INTERCONNECT; TEST; EXECUTE; COMPATIBLE; PRODUCT; MANUFACTURE; OSI; STANDARD; HIGH; ORDER; PERFORMANCE; CONTROL; OBSERVE; SERVICE; PRIMITIVE; INSTALLATION; LOWER; MONITOR; ACTUAL; TRANSMISSION; RECEPTION

Class Codes
International Classification (Main): H04L-029/14

File Segment: EPI;
DWPI Class: W01
Manual Codes (EPI/S-X): W01-A07G...

Alerting Abstract ...21) is provided at the higher level of the test installation. A performed type sub- test case is loaded from the test system. Based on the indication from the test system, the sub- test case is referred at the designated time . The described test is performed by appropriate device. The higher order tester processes the result of the described test. In...

35/69,K/51   (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2006 The Thomson Corporation. All rts. reserv.

0007805788 - Drawing available
WPI ACC NO: 1996-433262/ 199643
XRPX ACC No: N1996-365113
Test case control system using direct communication path to system under test - has processor which executes master procedure, which contains routines for displaying options to user for input selection
Patent Assignee: CENTIGRAM COMMUNICATIONS CORP (CENT-N)
Inventor: FITCH T M
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 5557539	A	19960917	US 1994258395	A	19940613	199643	B

Priority Applications (no., kind, date): US 1994258395 A 19940613

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5557539	A	EN	13	6	

Alerting Abstract US A
The system includes a communication path for communicating with a system under test (SUT), a display, while a master procedure is provided for displaying on the display any selected one of the test cases and for displaying user selectable options corresp to the hyper-links in the selected test case. The master procedure enables hyper-linked launching of each procedure corresp to user selected options and hyper-linked loading of

each file corresp to user selected options. The master procedure further enables user modification of selected ones of the stored files and storage of modified files in the memory.

A processor is configured to execute the number of procedures and to generate a number of signals. The processor including a transmitter that transmits the number of signals to the SUT via the communication path, and the processor including a receiver that receives a number of signals from the SUT via the communication path.

USE/ADVANTAGE - For testing telephony equipment contg voice mail, PBX etc systems. Permits test manager to set up and execute test procedures while accessing relevant database, document and test case information.

Title Terms/Index Terms/Additional Words: TEST; CASE; CONTROL; SYSTEM; DIRECT; COMMUNICATE; PATH; PROCESSOR; EXECUTE; MASTER; PROCEDURE; CONTAIN ; ROUTINE; DISPLAY; OPTION; USER; INPUT; SELECT

Class Codes
International Classification (Main): G06F-017/00

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-J08C

199643

Original Publication Data by Authority

Original Abstracts:
...a telephonic interface. The processor procedures include a master procedure and subprocedures for debugging the **test** **case** , retrieving and displaying documents, storing and retrieving database items, **test** **case** procedure development and editing, and test report generation. The processor procedures are all hyperlinked together so that the testing system can **call** any of the procedures at **specified** **times** in order to permit a user to read or modify database entries, documents and **test** **cases** when necessary. A method for testing an interactive voice messaging system includes steps for performing the **test** **case** control system of the present invention. The present apparatus and method are also applicable to...

Set	Items	Description
S1	1131	TESTCASE? OR CASE? ?(2N)(TEST OR TESTS OR TESTED OR TESTIN-G)
S2	16664	SIMULAT?R? ? OR SIMULATION? ?
S3	11411	BATCH? OR BATCHQUEUE?
S4	75	TESTDRIVE? OR TEST()DRIVE? ?
S5	6805	QUEUE? OR QUEU???
S6	463980	SOFTWARE? OR SOFT()WARE? ? OR APPLICATION? ? OR APP? ?
S7	759	S6(3N)(TEST OR TESTS OR TESTED OR TESTING OR TRIAL? ?)
S8	1238190	SPECIFIC OR SPECIFIED OR DESIGNATED OR SCHEDUL? OR APPOINT-??? OR PARTICULAR OR DEFINED OR DEFINITE OR STATED OR SELECTED
S9	1589130	DETERMINED OR DENOTED OR TARGETED OR CERTAIN OR CHOSEN OR - IDENTIFIED OR STIPULATED OR PRESCRIBED OR DECIDED OR SET OR G-IVEN
S10	899634	ESTABLISHED OR ARRANGED OR PREDESIGNATED OR PRESCHEDULED OR PREAPPOINTED OR PREDEFINED OR PRESTATED OR PRESELECTED OR PR-EDETERMINED
S11	59511	PRETARGETED OR PRECHOSEN OR PREIDENTIFIED OR PRESTIPULATED OR PREDECIDED OR PRESET OR PREESTABLISHED OR PREARRANGED OR P-RESPECIFIED
S12	165	PREPROGRAM? OR PRE()PROGRAM???? OR PRECONFIGURED OR PRE()C-ONFIGURED
S13	618453	FIXED
S14	166320	S8:S13(2W)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TI-MELINE?)
S15	73631	TIMED OR TIME()DEPENDENT OR TIMEDEPENDENT OR (TIMING OR TI-ME)(1W)CIRCUIT? OR TIMER? ?
S16	6130	S14:S15(7N)(EXECUTE? ? OR EXECUTION OR EXECUTING OR RUN OR RUNS OR RAN OR RUNNING)
S17	12035	S14:S15(7N)(EXERCIS? OR PERFORM? OR DEPLOY? OR LAUNCH? OR - ACTIVAT? OR ACTUAT? OR EVOK? OR EVOC? OR INVOK? OR INVOC? OR - ENABL? OR INABL?)
S18	25410	S14:S15(7N)(INITIALIS? OR INITIALIZ? OR IMPLEMENT? OR STAR-T??? OR BEGIN? ? OR BEGAN OR BEGUN OR COMMENC????? OR CALL? ? OR CALLED OR CALLING)
S19	8289	S14:S15(7N)(PROCESS OR PROCESSED OR PROCESSING OR PROCESSES OR HANDL???)
S20	0	TIMETRIGGER?
S21	1330	TRIGGER?(3N)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? - OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TIMELINE?)
S22	841	TRIGGER?(3N)(TIMED OR TIMEDEPENDENT OR TIMING OR TIMER? ?)
S23	631	(S1:S5 OR S7) AND S16:S22
S24	13	S23 AND S7
S25	11	S24 AND PY=1963:2001

25/9/2

06513607   **Image available**
DEVICE AND METHOD FOR ACTIVATING SAMPLE SOFTWARE AND STORAGE MEDIUM RECORDING CONTROL PROGRAM THEREFOR

PUB. NO.:   2000-099324 [JP 2000099324 A]
PUBLISHED: April 07, 2000 (20000407)
INVENTOR(s):   YASUDA YOSHIHARU
               KANEDA TOSHITAKA
APPLICANT(s): SHARP CORP
APPL. NO.:   10-273225 [JP 98273225]

ABSTRACT

PROBLEM TO BE SOLVED: To install program data without enciphering them, to /
 activate sample software on the **set** date and **time** and to confirm all /
functions by incorporating trial limit data for permitting the install of !
application program(AP) data and the activation of that program within the
date and time preset to the sample software.
SOLUTION: Concerning a storage medium 12, the computer of a central control :
part 8 reads the sample **software** , in which the **trial** limit data for :
limiting the trial of AP data and that program corresponding to the date
and time through a reading part 13. On the current date and time counted by
a time count part 7, a judging part 8a judges whether these data can be
tried or not. When the trial is disabled, it is reported by a reporting
part 2-1 but when the trial is enabled, an activating part 8b installs the
AP data in a previously provided program data buffer 11-2 and activates the
AP.

ABSTRACT

PROBLEM TO BE SOLVED: To automatically adjust the optional waiting time and
to facilitate execution of a **software** **test** by generating an interrupt
when the waiting time is reached by means of a virtual **timer** and
 starting a prescribed **process** .

SOLUTION: When the software 1 is simulated via a virtual computer, the
waiting time T that is set to make a **timer** acceleration calculation
device 3 **start**   **execution** of its prescribed process is detected to
decide whether the time T is longer than the prescribed threshold time. In
such a case, a virtual timer is prepared for every virtual computer and the
acceleration of the virtual timer is set to be 1 in the same way as a real
computer when it's decided that the minimum value of time T of the virtual
computer is smaller than its threshold. Then a timer interrupt is generated
and notified to each software 1 when the set value (time elapsed after
correction) of every virtual timer exceeds its prescribed value.

ABSTRACT

PROBLEM TO BE SOLVED: To prevent excessive load input to a test object
application program so as to automatically shorten time for train travel
simulation .

SOLUTION: A train operation control system for integrally supporting
passenger transportation service on the basis of the state of site
equipment such as a train diagram has a train travel simulator program 6,
an initialization value storage table 9, a processing table 10 for a
simulator and a processing table for a train operation control system. In
this train operation control system, the train diagram in read on the basis
of the initialization value to compute the number of trains to be formed,
the acceleration time width of an event generating periodic timer that
determines the acceleration of the simulator is computer from the number
of trains and the initialization value, and the timer is periodically
updated according to the acceleration time width. The maximum on-track
number of trains is previously registered, maximum load corresponding to a
simulation object is set, and an event over the maximum value is not
generated.

04744138   **Image available**
CONTROLLER WITH VARIABLE SPEED TIMER

ABSTRACT

PURPOSE: To improve the efficiency of the test of an application
program and to perform the test using an original parameter.

CONSTITUTION: This controller with a variable speed timer is provided with
a crystal oscillator 9 for generating reference clock signals, a frequency
dividing means 23 for frequency dividing the reference clock signal and
preparing prescribed time signals, a double speed value setting area 21 for
storing a double speed value required for executing a double speed
processing at the time of testing the application program, a system
timer preparation means 24 for executing the double speed processing

every time the time signals outputted from the frequency dividing means 23 are received and a system timer counter 22 for outputting the result of the double speed processing, that is, double speed reference time signals.

25/9/7

04174550   **Image available**
SYSTEM FOR SIMULATING TAPE END DETECTION IN MAGNETIC TAPE DEVICE

ABSTRACT

PURPOSE: To efficiently test software supporting a multi-volume form by detecting an EOT(end of tape) spuriously and generating an EOT detecting signal according to the pseudo EOT detection.

CONSTITUTION: A mode is made a pseudo EOT mode by a an MT control part 11 when a special command is imparted from a host device and a timer is started when a pseudo EOT condition specifying a time is set in the command. A check of whether the specified pseudo EOT condition (specified tape traveling amount from tape starting end, specified lapse of time , etc.) is realized or not is performed by comparing with the tape traveling amount indicated on a traveling amount meter 13 or the count value of the timer 14 by a pseudo EOT control part 12 when a normal MT control command is executed in the pseudo EOT mode. The EOT detecting signal is generated and sent to the host device by regarding as the pseudo EOT is detected by the MT control part 11 when the realization of the pseudo EOT condition is discriminated.
?

Set	Items	Description
S1	58314	TESTCASE? OR CASE? ?(2N)(TEST OR TESTS OR TESTED OR TESTING)
S2	3306611	SIMULAT?R? ? OR SIMULATION? ?
S3	209449	BATCH? OR BATCHQUEUE?
S4	1726	TESTDRIVE? OR TEST()DRIVE? ?
S5	128694	QUEUE? OR QUEU???
S6	7320445	SOFTWARE? OR SOFT()WARE? ? OR APPLICATION? ? OR APP? ?
S7	106850	S6(3N)(TEST OR TESTS OR TESTED OR TESTING OR TRIAL? ?)
S8	7010983	SPECIFIC OR SPECIFIED OR DESIGNATED OR SCHEDUL? OR APPOINT-??? OR PARTICULAR OR DEFINED OR DEFINITE OR STATED OR SELECTED
S9	9731644	DETERMINED OR DENOTED OR TARGETED OR CERTAIN OR CHOSEN OR - IDENTIFIED OR STIPULATED OR PRESCRIBED OR DECIDED OR SET OR G-IVEN
S10	1282239	ESTABLISHED OR ARRANGED OR PREDESIGNATED OR PRESCHEDULED OR PREAPPOINTED OR PREDEFINED OR PRESTATED OR PRESELECTED OR PR-EDETERMINED
S11	22930	PRETARGETED OR PRECHOSEN OR PREIDENTIFIED OR PRESTIPULATED OR PREDECIDED OR PRESET OR PREESTABLISHED OR PREARRANGED OR P-RESPECIFIED
S12	5141	PREPROGRAM? OR PRE()PROGRAM???? OR PRECONFIGURED OR PRE()C-ONFIGURED
S13	703377	FIXED
S14	151957	S8:S13(2W)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR TI-MELINE?)
S15	299585	TIMED OR TIME()DEPENDENT OR TIMEDEPENDENT OR (TIMING OR TI-ME)(1W)CIRCUIT? OR TIMER? ?
S16	3545	S14:S15(7N)(EXECUTE? ? OR EXECUTION OR EXECUTING OR RUN OR RUNS OR RAN OR RUNNING)
S17	15708	S14:S15(7N)(EXERCIS? OR PERFORM? OR DEPLOY? OR LAUNCH? OR -

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              ACTIVAT? OR ACTUAT? OR EVOK? OR EVOC? OR INVOK? OR INVOC? OR -
              ENABL? OR INABL?)
S18      8604    S14:S15(7N)(INITIALIS? OR INITIALIZ? OR IMPLEMENT? OR STAR-
              T??? OR BEGIN? ? OR BEGAN OR BEGUN OR COMMENC????? OR CALL? ?
              OR CALLED OR CALLING)
S19     17329    S14:S15(7N)(PROCESS OR PROCESSED OR PROCESSING OR PROCESSES
              OR HANDL???)
S20         1    TIMETRIGGER?
S21      5358    TRIGGER?(3N)(TIME OR TIMES OR TIMEFRAME? OR TIMEINTERVAL? -
              OR TIMEPERIOD? OR TIMECYCLE? OR TIMESCHEDUL? OR TIMETABLE? OR
              TIMELINE?)
S22      1074    TRIGGER?(3N)(TIMED OR TIMEDEPENDENT OR TIMING OR TIMER? ?)
S23      9243    (S1:S5 OR S7) AND S16:S22
S24      2767    S23 AND S6
S25       146    S23 AND S1
S26       203    S23 AND S7
S27        41    S26 AND S16
S28        23    S25 AND S16
S29        58    S27:S28
S30        12    S29/2002:2006
S31        46    S29 NOT S30
S32        28    RD  (unique items)
S33    423373    S6(5N)DEVELOP????
S34       216    S23 AND S33
S35       166    S34 AND S1:S4
S36        38    S35/2004:2006
S37       123    S35 NOT (S36 OR S29)
S38        86    RD  (unique items)
S39        22    S34 AND S5
S40        14    S39/2002:2006
S41         7    S39 NOT (S40 OR S37 OR S29)
S42         7    S41 NOT S35
S43         5    RD  (unique items)
```

? t32/7/1-2,4,6,16,18,24

32/7/1   (Item 1 from file: 2)

08122907   INSPEC Abstract Number: C2002-01-6110B-054
   Title: Compact trace generation and power measurement in software
emulation
   Author(s): Wolf, F.; Kruse, J.; Ernst, R.
   Author Affiliation: Inst. ffir Datenverarbeitungsanlagen, Technische
Univ. Braunschweig, Germany
   Journal: Proceedings of the SPIE - The International Society for Optical
Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA)
vol.4228   p.97-108
   Publisher: SPIE-Int. Soc. Opt. Eng,
   Publication Date: 2000 Country of Publication: USA
   CODEN: PSISDG   ISSN: 0277-786X
   SICI: 0277-786X(2000)4228L.97:CTGP;1-Q
   Material Identity Number: C574-2001-082
   U.S. Copyright Clearance Center Code: 0277-786X/00/$15.00
   Conference Title: Design, Modeling, and Simulation in Microelectronics
   Conference Sponsor: SPIE; Nanyang Technol. Univ
   Conference Date: 28-30 Nov. 2000   Conference Location: Singapore
   Language: English   Document Type: Conference Paper (PA); Journal Paper
(JP)
   Treatment: Theoretical (T)
   Abstract: Evaluation boards are popular as prototyping platforms in
embedded software development. They often are preferred over simulation
 to avoid modeling effort and simulation times as well as over complete
hardware prototypes to avoid development cost. Evaluation boards provide
accurate timing results as long as the main architecture parameters match
the target hardware system. For larger processors, this is often not the
case since the cache and main memory architectures might differ. Another
problem is the lack of observability of the software execution. Pin-Out
versions of processors with improved observability are expensive (so are
in-circuit emulators) and not always available, and on-chip processor test
 support requires software adaptation. A particular problem arises when
trying to verify the running time bounds of embedded software such as
required for hard real-time systems. Here, formal analysis approaches have
been proposed which require segment-wise execution of a program under
investigation. Another problem is the accurate analysis of processor power
consumption for different execution paths. The paper presents an approach
to fast acquisition of compact timed   execution traces with instruction
cycle accurate power samples on commercial evaluation kits. Global system
modeling abstracts the environment to a set of parameters that is included
in the software under investigation for segment-wise, real- time
 execution. Trigger points write source code line numbers and energy
samples to the address and data bus where they are read by a logic state
analyzer. Experiments show that the application of trigger points avoids
the acquisition of long, complete traces on sophisticated, dedicated
prototyping platforms as in previous work while more accurate execution
time and power consumption can be delivered. (12 Refs)
   Subfile: C

32/7/2   (Item 2 from file: 2)

07873169   INSPEC Abstract Number: C2001-04-4220-047
   Title: Generating test   cases for a timed I/O automaton model
   Author(s): Higashino, T.; Nakata, A.; Taniguchi, K.; Cavalli, A.R.

Author Affiliation: Dept. of Inf. & Math. Sci., Osaka Univ., Japan
Abstract: Recently various real-time communication protocols have been proposed. In this paper, first, we propose a timed I/O automaton model so that we can simply specify such real-time protocols. The proposed model can handle not only time but also data values. Then, we propose a conformance testing method for the model. In order to trace a test sequence (I/O sequence) on the timed I/O automaton model, we need to execute each I/O action in the test sequence at an adequate execution timing which satisfies all timing constraints in the test sequence. However, since outputs are given from IUTs and uncontrollable, we cannot designate their output timing in advance. Also their output timing affects the executable timing for the succeeding I/O actions in the test sequence. Therefore, in general, the executable timing of each input action in a test sequence can be specified by a function of the execution time of the preceding I/O actions. In this paper, we propose an algorithm to decide efficiently whether a given test sequence is executable. We also give an algorithm to derive such a function from an executable test sequence automatically using a technique for solving linear programming problems, and propose a conformance testing method using those algorithms. (16 Refs)
Subfile: C

32/7/4   (Item 4 from file: 2)

07207475   INSPEC Abstract Number: C1999-05-6150C-006
Title: FASTEST: a practical low-complexity algorithm for compile-time assignment of parallel programs to multiprocessors
Author(s): Yu-Kwong Kwok; Ahmad, I.
Author Affiliation: Dept. of Electr. & Electron. Eng., Hong Kong Univ., Hong Kong
Abstract: In the area of parallelizing compilers, considerable research has been carried out on data dependency analysis, parallelism extraction, as well as program and data partitioning. However, designing a practical, low complexity scheduling algorithm without sacrificing performance remains a challenging problem. A variety of heuristics have been proposed to generate efficient solutions but they take prohibitively long execution times for moderate size or large problems. In this paper, we propose an algorithm called FASTEST (Fast Assignment and Scheduling of Tasks using an Efficient Search Technique) that has O(e) time complexity, where e is the number of edges in the task graph. The algorithm first generates an initial

solution in a short time and then refines it by using a simple but robust random neighborhood search. We have also parallelized the search to further lower the time complexity. We are using the algorithm in a prototype automatic parallelization and scheduling tool which compiles sequential code and generates parallel code optimized with judicious scheduling. The proposed algorithm is evaluated with several application programs and outperforms a number of previous algorithms by generating parallelized code with shorter **execution** times, while taking dramatically shorter **scheduling** times . The FASTEST algorithm generates optimal solutions for a majority of the **test** **cases** and close-to-optimal solutions for the rest. (26 Refs)
  Subfile: C
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  32/7/6   (Item 6 from file: 2)
DIALOG(R)File   2:INSPEC
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06939728   INSPEC Abstract Number: C9807-4240-011
  Title: Determining optimal testing times for Markov chain usage models [software   testing]
  Author(s): Semmel, G.S.; Linton, D.G.
  Author Affiliation: NASA, Kennedy Space Center, FL, USA
  Conference Title: Proceedings. IEEE Southeastcon '98. `Engineering for a New Era' (Cat. No.98CH36170)   p.1-4
  Publisher: IEEE, New York, NY, USA
  Publication Date: 1998 Country of Publication: USA   xiv+416 pp.
  ISBN: 0 7803 4391 3   Material Identity Number: XX98-01252
  U.S. Copyright Clearance Center Code: 0 7803 4391 3/98/$10.00
  Conference Title: Proceedings IEEE Southeastcon '98 `Engineering for a New Era'
  Conference Sponsor: IEEE Region 3; IEEE Orlando Sect.; IEEE Orlando Student Branch; Univ. Central Florida, Coll. Eng
  Conference Date: 24-26 April 1998   Conference Location: Orlando, FL, USA
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Theoretical (T)
  Abstract: Statistical **software** **testing** presents two difficulties for the tester: (1) establishing accurate user profiles (i.e. usage probabilities), and (2) incurring lengthy test times. An algorithm, named the frequency count method (FCM), is developed which addresses both difficulties simultaneously. FCM finds usage probabilities within predetermined ranges and concurrently minimizes the amount of testing time. First, FCM randomly generates a large number of matrices for a given Markov chain with constrained usage probabilities. For each one-step transition matrix associated with the given Markov chain usage model, FCM simulates the steps of the chain. FCM flags the usage matrix which requires the minimum expected amount of testing time (assuming no failures) and ensures theoretical and calculated stationary probability values are within some preset precision. Thus, by generating test sequences from the usage probabilities of the flagged matrix, the expected minimum statistical testing time is achieved. This minimum time is optimal with respect to the transition probability ranges and the **given** **execution** **times** . Employing a 5-state usage model with numerical values for the transition probability bounds and code execution times, the FCM algorithm is illustrated and the expected minimum testing time is calculated. (4 Refs)
  Subfile: C
  Copyright 1998, IEE

  32/7/16   (Item 1 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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05272642   E.I. No: EIP99044635000
   Title: FASTEST: A practical low-complexity algorithm for compile-time assignment of parallel programs to multiprocessors

   Author: Kwok, Yu-Kwong; Ahmad, Ishfaq
   Corporate Source: Univ of Hong Kong, Hong Kong, Hong Kong
   Abstract: In the area of parallelizing compilers, considerable research has been carried out on data dependency analysis, parallelism/extraction, as well as program and data partitioning. However, designing a practical, low complexity scheduling algorithm without sacrificing performance remains a challenging problem. A variety of heuristics have been proposed to generate efficient solutions but they take prohibitively long execution times for moderate size or large problems. In this paper, we propose an algorithm called FASTEST (Fast Assignment and Scheduling of Tasks using an Efficient Search Technique) that has O(e) time complexity, where e is the number of edges in the task graph. The algorithm first generates an initial solution in a short time and then refines it by using a simple but robust random neighborhood search. We have also parallelized the search to further lower the time complexity. We are using the algorithm in a prototype automatic parallelization and scheduling tool which compiles sequential code and generates parallel code optimized with judicious scheduling. The proposed algorithm is evaluated with several application programs and outperforms a number of previous algorithms by generating parallelized code with shorter execution times, while taking dramatically shorter scheduling times . The FASTEST algorithm generates optimal solutions for a majority of the test cases and close-to-optimal solutions for the rest. (Author abstract) 26 Refs.

   32/7/18   (Item 3 from file: 8)

04928996   E.I. No: EIP98024046146
   Title: Parallel algorithm for compile-time scheduling of parallel programs on multiprocessors
   Author: Kwok, Yu-Kwong; Ahmad, Ishfaq
   Corporate Source: Hong Kong Univ of Science and Technology, Hong Kong, Hong Kong
   Abstract: In this paper, we propose a parallel randomized algorithm, called Parallel Fast Assignment using Search Technique (PFAST), for scheduling parallel programs represented by directed acyclic graphs (DAGs) during compile-time. The PFAST algorithm has O(e) time complexity where e is the number of edges in the DAG. This linear-time algorithm works by first generating an initial solution and then refining it using a parallel random search. Using a prototype computer-aided parallelization and

scheduling tool called CASCH, the algorithm is found to outperform numerous previous algorithms while taking dramatically smaller execution times. The distinctive feature of this research is that, instead of simulations , our proposed algorithm is evaluated and compared with other algorithms using the CASCH tool with real applications running on the Intel Paragon. The PFAST algorithm is also evaluated with randomly generated DAGs for which optimal schedules are known. The algorithm generated optimal solutions for a majority of the test   cases and close-to-optimal solutions for the others. The proposed algorithm is the fastest scheduling algorithm known to us and is an attractive choice for scheduling under running   time constraints. (Author abstract) 22 Refs.

   32/7/24   (Item 4 from file: 34)

Title: ARCHITECTURAL TIMING VERIFICATION OF CMOS RISC PROCESSORS
Author(s): BOSE P; SURYA S
Corporate Source: IBM CORP,DIV RES,THOMAS J WATSON RES CTR,POB 218/YORKTOWN
    HTS//NY/10598; IBM CORP,DIV SYST TECHNOL &
    ARCHITECTURE/AUSTIN//TX/78758
Abstract: We consider the problem of verification and testing of
    architectural timing models ('' timers '') coded to predict
    cycles-per-instruction (CPI) performance of advanced CMOS superscalar
    (RISC) processors. Such timers are used for pre-hardware performance
     analysis and prediction. As such, these software models play a vital
    role In processor performance tuning as well as application-based
    competitive analysis, years before actual product availability. One of
    the key problems facing a designer, modeler, or application analyst who
    uses such a tool is to understand how accurate the model is, in terms
    of the actual design. in contrast to functional simulators , there is
    no direct way of testing timers in the classical sense, since the
    ''correct'' execution time (in cycles) of a program on the machine
    model under test is not directly known or computable from equations,
    truth tables, or other formal specifications. Ultimate validation (or
    invalidation) of such models can be achieved after actual hardware
    availability, by direct comparisons against measured performance.
    However, deferring validation solely to that stage would do little to
    achieve the overall purpose of accurate pre-hardware analysis, tuning,
    and projection. We describe a multilevel validation method which has
    been used successfully to transform evolving timers into highly
    accurate pre-hardware models. In this paper, we focus primarily on the
    following aspects of the methodology: a) establishment of cause-effect
    relationships in terms of model defects and the associated fault
    signatures; b) derivation of application -based test loop kernels to
    verify steady-state (periodic) behavior of pipeline flow, against
    analytically predicted signatures; and c) derivation of synthetic test
      cases to verify the ''core'' parameters characterizing the
    pipeline-level machine organization as implemented in the timer
    model. The basic tenets of the theory and its application are described
    in the context of an example processor, comparable in complexity to an
    advanced member of the PowerPC(TM) 6XX processor family.
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? t38/7/8,10,18-19,25

38/7/8   (Item 8 from file: 2)
DIALOG(R)File   2:INSPEC
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07650328   INSPEC Abstract Number: C2000-08-6110F-053
  Title: From timed **scenarios to SDL: specification,** implementation **and**
testing of real-time systems
  Author(s): En-Nouaary, A.; Dssouli, R.; Khendek, F.
  Author Affiliation: Dept. d'Inf. et de Recherche Oper., Montreal Univ.,
Que., Canada
  Conference Title: SDL '99. The Next Millennium. Proceedings of the Ninth
SDL Forum   p.67-80
  Editor(s): Dssouli, R.; Bochmann, G.V.; Lahav, Y.
  Publisher: Elsevier Science, Amsterdam, Netherlands
  Publication Date: 1999 Country of Publication: Netherlands   xii+489
pp.
  ISBN: 0 444 50228 9   Material Identity Number: XX-1999-03034
  Conference Title: Proceedings of Ninth SDL'99 Forum. The Next Millennium
  Conference Date: 21-25 June 1999   Conference Location: Montreal, Que.,
Canada
  Language: English   Document Type: Conference Paper (PA)
  Treatment: Practical (P)
  Abstract: Nowadays, software systems are increasingly involved in
safety-critical systems such as patient monitoring systems and air traffic
control systems. Moreover, we witness the rapid **development** and
deployment of new **applications** such as multimedia systems. The behavior
of these systems are **time - dependent** . To be simulated, validated and
implemented , real time systems must be specified in a formal description
technique (FDT). We propose a methodology to specify, implement, and test
real time systems. A system is first specified as a set of timed scenarios.
These scenarios are integrated (via the tool REST (S.S. Some et al., 1995))
to obtain a set of timed finite state machines (TFSM), a variant of timed
automata (R. Alur and D. Dill, 1994). The resulting TFSMs are translated
into SDL. After being validated, the SDL specification is used to generate
automatically a partial implementation which is completed by the user. This
implementation must be tested to assess its conformance to its
specification. Timed **test cases** used to achieve this goal are generated
from the TFSMs derived using REST. (21 Refs)
  Subfile: C
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38/7/10   (Item 10 from file: 2)
DIALOG(R)File   2:INSPEC
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07430131   INSPEC Abstract Number: B2000-01-6210Q-003, C2000-01-5640-049
  Title: INAP conformance test system development and verification using IUT
simulator
  Author(s): Seongyong Bae; Hyunjoo Bae; Sehyeong Cho
  Author Affiliation: Electron. & Telecommun. Res. Inst., Daejeon, South
Korea
  Conference Title: IEEE GLOBECOM 1998 (Cat. NO. 98CH36250)   Part vol.6
p.3356-61 vol.6
  Publisher: IEEE, Piscataway, NJ, USA
  Publication Date: 1998 Country of Publication: USA   6 vol.
(lxxii+lii+3773) pp.
  ISBN: 0 7803 4984 9   Material Identity Number: XX-1999-01290
  U.S. Copyright Clearance Center Code: 0 7803 4984 9/99/$10.00
  Conference Title: IEEE GLOBECOM 1998
  Conference Sponsor: IEEE; IEEE Commun. Soc.; ICC GLOBECOM
  Conference Date: 8-12   Nov.   1998   Conference   Location:
Sydney,NSW,Australia

    Abstract: This paper describes the design and implementation of an intelligent network application protocol (INAP) conformance tester. The INAP conformance test system consists of the abstract test suite (ATS) generation function, the test preparation function, the test execution function, and test analysis function. For rapid development and credibility of the test system, we made use of commercially available CASE **software** and a protocol tester. The **developed** test system is verified by using an IUT (implementation under test) **simulator** . Verification of the test system comprises ATS verification and the test execution manager verification. Verification of the ATS includes correcting the logical and syntactic errors generated during running the executable test suite (ETS) against the IUT **simulator** . In the test execution manager verification, various manager functions such as **test** **case** selection and **timer** **processing** are examined if they operate properly. While it is practically impossible to guarantee the perfection of the test system, the use of IUT **simulator** greatly enhances the credibility of the test system. The test system has been used for testing an IP system, an SCP system, and an SSP system. (20 Refs)
    Subfile: B C

38/7/18 (Item 18 from file: 2)

    Title: Promises and perils of production QMF (Query Management Facility)
    Author(s): Sayles, J.
    Abstract: Asking DB2 shops about IBM's Query Management Facility (QMF) for ad hoc query and reporting, produces different perspectives. Some shops strictly limit QMF use to an **application development** tool for the programming staff. Others permit some user access through QMF to certain types of DB2 data; still others allow QMF activity only at **specific times** of day or through **batch processing** jobs. How does one implement or enhance QMF use in a low-risk manner? How can one effectively establish control mechanisms while maximizing return on investment? The author addresses these questions as well as concerns regarding production QMF use in a DB2 or SQL/DS environment. He believes that QMF is a fine report writer and ad hoc query product. In fact, many issues he raises (particularly in the areas of performance and security) have little to do with QMF, but are really general problems associated with SQL, relational databases, and ad hoc data access. (0 Refs)
    Subfile: C

38/7/19 (Item 19 from file: 2)

    Title: An application generator for a family of real-time monitor and control systems
    Author(s): Benaya, T.; Yehudai, A.
    Author Affiliation: Tel-Aviv Univ., Israel

Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1990 Country of Publication: USA   xiii+574 pp.
ISBN: 0 8186 2041 2
U.S. Copyright Clearance Center Code: CH2867-0/90/0000-0274$01.00
Conference Sponsor: IEEE; Inf. Processing Assoc. Israel
Conference Date: 8-10 May 1990   Conference Location: Tel-Aviv, Israel
Language: English   Document Type: Conference Paper (PA)
Treatment: Practical (P)

Abstract: An application generator (AG) for a family of real-time monitor
and control system (RTMCS) is presented. The input to the AG is a system
specification of a desired RTMC system, and the output is an Ada program
for the specified system (the target system). The system specification of a
desired RTMC system is defined with the aid of an interactive menu-driven
program. After checking the specification for internal inconsistencies and
commissions, the AG generates Ada code for the specified target system. The
generated code can then be compiled and linked to produce either an
operational target system or a simulation of the target system. The
family of applications for which this AG was developed includes
real-time systems which receive data from the real world, based on
asynchronous interrupts; process the data by performing
transformations, analysis and timed response in the form of local
displays, alarms and remote control; and control the environment by means
of both operator and automatic control. (13 Refs)
Subfile: C

38/7/25   (Item 25 from file: 2)
DIALOG(R)File   2:INSPEC

02282940   INSPEC Abstract Number: B79002666, C79002265
Title: Simulation of microprocessor in development of software for
measurements of the peak electrical energy loading
Author(s): Zumer, V.; Gregorcic, M.
Author Affiliation: Electrotech. Review, Ljubljana, Yugoslavia
Journal: Elektrotehniski Vestnik   vol.45, no.1   p.11-14
Publication Date: Jan.-Feb. 1978 Country of Publication: Yugoslavia
CODEN: ELVEA2 ISSN: 0013-5852
Language: Slovenian   Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The   simulation   is based on an interpreting principle, which
accepts an input data program for the microprocessor in machine code and
also the other specific data required by the program. The result of
simulation   is a printed list of data from the memory, accumulators and
registers of the microprocessor. With the aid of the microprocessor it is·
very simple to realize low cost but accurate apparatus for measurements of
used electrical energy. Through PIA the data of used energy from different
pick-off points are entered, and are processed in definite time
intervals. (4 Refs)
Subfile: B C
? t38/7/28,30,32,35-36,39,42

38/7/28   (Item 3 from file: 6)
DIALOG(R)File   6:NTIS

2023844 NTIS Accession Number: N19970020573/XAB
   Unsteady Multidimensional Simulations of the Structure and Dynamics of
Flames
Kailasanath, K. ; Patnaik, G. ; Oran, E. S.
Naval Research Lab., Washington, DC.
Corp. Source Codes: 000927000; NS999791
May 97   6p
Languages: English
Journal Announcement: GRAI9723; STAR3507

The primary objective of our research is to develop an understanding of the differences in the structure, stability, dynamics and extinction of flames in earth gravity and in microgravity environments. Numerical simulations , in which the various physical and chemical processes can be independently controlled, can significantly advance our understanding of these differences. Therefore, our approach is to use detailed **time - dependent** , multidimensional, multispecies numerical models to **perform** carefully designed computational experiments. Some of these computational experiments are also complementary to physical experiments performed under the Microgravity Combustion Science Program. In this report, we provide a brief summary of our research since the last microgravity combustion workshop. The two major projects we have been working on are: (1) the **development** and **application** of a three-dimensional, time-dependent flame model, and (2) a study of the effects of gravity on flame-vortex interactions. A state-of-the-art parallel flame code, FLAME3D, has been developed and used to simulate the three-dimensional cellular structure of lean hydrogen flames. The results from the **simulations** have been compared to our previous two-dimensional **simulations** to understand the role of three-dimensionality. This is discussed below in some detail after a brief discussion of the flame code. The second project deals with flame-vortex interactions under different gravitational environments such as zero, upward and downward Earth gravity. These numerical experiments are complementary to the physical experiments of Driscoll et al reported elsewhere in these proceedings.

38/7/36   (Item 7 from file: 8)

05899659   E.I. No: EIP01416673126
   Title: VirtualExplorer: A plugin-based virtual reality framework
   Author: Kuester, F.; Hamann, B.; Joy, K.I.
   Corporate Source: Ctr. Image Proc. Integrated Comp. Department of
Computer Science University of California, Davis, CA 95616-8562, United
States
   Conference Title: Stereoscopic Displays and Virtual Reality Systems VIII
   Conference Location: San Jose, CA, United States   Conference Date:
20010122-20010125
   Sponsor: SPIE
   E.I. Conference No.: 58392
   Source: Proceedings of SPIE - The International Society for Optical
Engineering v 4297 2001. p 436-442
   Publication Year: 2001
   CODEN: PSISDG   ISSN: 0277-786X
   Language: English
   Document Type: CA; (Conference Article)   Treatment: A; (Applications)
   Journal Announcement: 0110W2
   Abstract: This paper introduces VirtualExplorer, a customizable
plugin-based virtual reality framework for immersive scientific data
visualization, exploration and geometric modeling. The framework is
layered on top of a run-time plugin system and reconfigurable virtual user
interface and provides a variety of plugin components. The system provides
access to scene-graph-based APIs, including Performer and OpenInventor,
direct OpenGL support for visualization of time-critical data as well as
collision and generic device managers. Plugins can be loaded, disabled,
enabled or unloaded at any time , triggered either through pre-defined
events or through an external Python-based interface. The virtual user
interface uses pre-defined geometric primitives that can be customized to
meet application-specific needs. The entire widget set can be
reconfigured dynamically on a per-widget basis or as a whole through a
style manager. The system is being developed with a variety of
application areas in mind, but its main emphasis is on user-guided data
exploration and high-precision engineering design. 18 Refs.

38/7/39   (Item 10 from file: 8)

05350396   E.I. No: EIP99094766037
   Title: INAP conformance test system development and verification using
IUT simulator
   Author: Bae, Seongyong; Bae, Hyunjoo; Cho, Sehyeong
   Corporate Source: Electronics and Telecommunications Research Inst,
Taejon, South Korea
   Conference Title: Proceedings of the IEEE GLOBECOM 1998 - The Bridge to
the Global Integration
   Conference   Location: Sydney,   NSW,   Aust   Conference   Date:
19981108-19981112
   Sponsor: IEEE Communications Society; Telstra; ERICSSON; SIEMENS; et al.
   E.I. Conference No.: 55358
   Source: Conference Record / IEEE Global Telecommunications Conference v 6
1998. p 3356-3361
   Publication Year: 1998
   CODEN: CRIEET
   Language: English
   Document Type: JA; (Journal Article)   Treatment: T; (Theoretical)
   Journal Announcement: 9910W2
   Abstract: This paper describes the design and implementation of an

Intelligent Network Application Protocol(INAP) conformance tester. The INAP
conformance test system consists of the Abstract Test Suite(ATS) generation
function, the test preparation function, the test execution function, and
test analysis function. For rapid development and credibility of the test
system, we made use of commercially available CASE **software** and a
protocol tester. The **developed** test system is verified by using an
IUT(Implementation Under Test) **simulator** . Verification of the test system
comprises ATS verification and the test execution manager verification.
Verification of the ATS includes correcting the logical and syntactic
errors generated during running the Executable Test Suite(ETS) against the
IUT **simulator** . In the test execution manager verification, various
manager functions such as **test** **case** selection and **timer** **processing**
are examined if they operate properly. While it is practically impossible
to guarantee the perfection of the test system, the use of IUT **simulator**
greatly enhances the credibility of the test system. The test system has
been used for testing an IP system, an SCP system, and an SSP system.
(Author abstract) 20 Refs.

 38/7/42   (Item 13 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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04019146   E.I. No: EIP94122493807
   Title: Timed   temporal   logic   framework   for   designing   real-time
applications
   Author: Ionescu, Dan
   Corporate Source: Univ of Ottawa, Ottawa, Ont, Can
   Conference Title: Proceedings of the IFIP 13th World Computer Congress.
Part 1 (of 3)
   Conference Location: Hamburg, Ger   Conference Date: 19940828-19940902
   E.I. Conference No.: 21456
   Source: IFIP Transactions A: Computer Science and Technology n A-51 1994.
p 322-329
   Publication Year: 1994
   CODEN: ITATEC   ISSN: 0926-5473
   Language: English
   Document Type: MC; (Monograph Chapter)   Treatment: G; (General Review);
T; (Theoretical)
   Journal Announcement: 9502W3
   Abstract: **Developing** **applications** for systems whose states change in
response to the occurrence of events and satisfy, time restrictions as
well, it proved to be a very delicate task. A framework for modeling,
analyzing and designing such systems is introduced in this paper, and
procedures for the reachability analysis and synthesis are developed. A
timed temporal logic is **implemented** and an example illustrates the
theoretical approach. (Author abstract) 12 Refs.

02072300   Genuine Article#: JY701   Number of References: 19
Title: OPTIMAL AIR-POLLUTION CONTROL STRATEGIES - A CASE-STUDY
Author(s): FINZI G; GUARISO G
Corporate Source: POLITECN MILAN,DEPT ELECTR,CTR ENVIRONM COMP SCI,VIA
    PONZIO 34-5/I-20133 MILAN//ITALY/
Journal: ECOLOGICAL MODELLING, 1992, V64, N2-3 (OCT 31), P221-239
ISSN: 0304-3800
Language: ENGLISH   Document Type: ARTICLE

Abstract: Air pollution can be controlled at a regional level in several
    different ways, such as emission standards, taxes, permits, etc. The
    European Community decided to set standards on environmental quality,
    namely on the distribution of pollutant concentrations measured at
    ground level. This paper deals with the problem of evaluating the
    trade-offs between such ambient standards and pollution abatement
    costs. For this purpose, a two-objective linear program is formulated
    and solved for a 300 km2 region in northern Italy, using a simulation
    model to evaluate the effects of each pollution source. The software
    developed forms the basis of a more complete decision support system
    for this type of complex problem. Its structure and components are
    described in detail.
...Abstract: program is formulated and solved for a 300 km2 region in
    northern Italy, using a simulation model to evaluate the effects of
    each pollution source. The software   developed forms the basis of a
    more complete decision support system for this type of complex...
...Research Fronts: PROGRAMMING; STOCHASTIC CHOICE THEORY)
  90-6007 001   (MULTIOBJECTIVE PROGRAMMING; MULTISTAGE MULTIPLE OBJECTIVE
    DECISION-MAKING PROBLEMS; SCHEDULING UNIT PROCESSING   TIME JOBS)
? t38/7/79

 15047437   PASCAL No.: 01-0205183
 Planning agents in JAMES
 Agents in modeling and simulation : exploiting the metaphor
 SCHATTENBERG Bernd; UHRMACHER Adelinde M
 UHRMACHER Adelinde M, ed; FISHWICK Paul A, ed; ZEIGLER Bernard P, ed
 Faculty of Computer Science, University of Ulm, 89081 Ulm, Germany;
Computer Science Department, University of Rostock, 18059 Rostock, Germany
 University of Rostock, 18051 Rostock, Germany; University of Florida,
Gainesville, FL 32611, United States; University of Arizona, Tucson, AZ
85721-0104, United States
 Journal: Proceedings of the IEEE, 2001, 89 (2) 158-173
 ISSN: 0018-9219 CODEN: IEEPAD Availability: INIST-222;
354000093935300030
 No. of Refs.: 62 ref.
 Document Type: P (Serial) ; A (Analytic)
 Country of Publication: United States
 Language: English

 Testing is an obligatory step in developing multiagent systems. For
testing multiagent systems in virtual, dynamic environments, simulation
systems are required that support a modular declarative construction of
experimental frames, that facilitate the embeddence of a variety of agent
architectures and that allow an efficient parallel, distributed execution.
We introduce the system JAMES (A Java-based agent modeling environment for
 simulation). In JAMES, agents and their dynamic environment are modeled
as reflective, time - triggered state automata. Its possibilities to
compose experimental frames based on predefined components, to express
temporal interdependencies, to capture the phenomenon of proactiveness and

reflectivity of agents are illuminated by experiments with planning agents. The underlying planning system is a general-purpose system, about which no empirical results exist besides traditional static benchmark tests. We analyze the interplay between heuristics for selecting goals, viewing range, commitment strategies, explorativeness, and trust in the persistence of the world and uncover properties of the agent, the planning engine, and the chosen test scenario: TILEWORLD.

? t43/7/1

43/7/1   (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
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03910040   INSPEC Abstract Number: C87042795
  Title: The selection of a servicing discipline in a multiterminal
conversational information retrieval system
  Author(s): Kavalerchik, B.Ya.
  Journal: Avtomatika i Vychislitel'naya Tekhnika   vol.20, no.4   p.
58-64
  Publication Date: 1986 Country of Publication: USSR
  CODEN: AVYTAK ISSN: 0132-4160
  Translated in: Automatic Control and Computer Sciences   vol.20, no.4
p.54-9
  Publication Date: 1986   Country of Publication: USA
  CODEN: ACCSCE   ISSN: 0146-4116
  U.S. Copyright Clearance Center Code: 0146-4116/86/$20.00
  Language: English   Document Type: Journal Paper (JP)
  Treatment: Practical (P)

  Abstract: The   choice   of   the request service discipline in the
 development   of a software for conversational IRS in automatic control
systems is investigated with a view to achieving a rapid system response at
a minimum resource utilization rate. A service procedure with two queues
is suggested; the requests requiring access to the automatic control
system's information base are processed sequentially, while functional
requests ('leafing' multipage reference materials, receiving instructions,
etc.) are processed after preset periods of time . The characteristics
of the queuing system are evaluated and the applicability range defined.
The importance of the psychological factor in the choice of service
discipline is underscored and the specifications of the design of the
respective software described. A conversational IRS developed according
to this scheme is in operation at several computer centers. (10 Refs)
  Subfile: C

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Timed multitasking for real-time embedded software

Jie Liu Lee, E.A.
Palo Alto Res. Center, CA, USA;

Abstract
An event-triggered programming model, timed multitasking, is introduced that also takes approach to real-time programming but controls timing properties through deadlines and time triggers.

Index Terms
Inspec
  Controlled Indexing
  computerised control   embedded systems   multiprogramming

  Non-controlled Indexing
  real-time embedded software   real-time programming   timed multitasking
Author Keywords
Not Available

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Abstract | Full Text: PDF (757)

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    On page(s): 250- 262, Volume: 12, Issue: 2, March 2004
    Abstract | Full Text: PDF (720)

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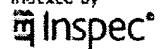
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12th IEEE International Workshop on Rapid System Prototyping (RSP'01) p. 0155

Model Based Testing in Evolutionary Software Development

Alexander Pretschner, Technische Universität München
Heiko Lotzbeyer, Technische Universität München
Jan Philipps, Technische Universität München

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http://doi.ieeecomputersociety.org/10.1109/IWRSP.2001.933854

Abstract

Abstract: The spiraling nature of evolutionary software development processes produces executable parts of the system at the end of each loop. We argue that these parts should consist not only of programming language code, but of executable graphical system models. As a main benefit of the use of more abstract, yet formal, modeling languages, we present a method for model based test sequence generation for reactive systems on the grounds of Constraint Logic Programming and its implementation in the CASE tool AutoFocus.Keywords. Cleanroom SW Engineering, Constraint Logic Programming, Extreme Programming, Incremental Development, Rapid Prototyping, Reactive Systems, Test Case Generation.

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Citation: Alexander Pretschner, Heiko Lotzbeyer, Jan Philipps, "Model Based Testing in Evolutionary Software Development," *rsp*, p. 0155, 12th IEEE International

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Workshop on Rapid System Prototyping (RSP'01), 2001.

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Second IEEE International Symposium on Object-Oriented Real-Time Distributed Computing p. 75

Applying Use Cases for the Requirements Validation of Component-Based Real-Time Software

Wolfgang Fleisch, University of Stuttgart

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Abstract

Component-based software development is a promising way to improve quality, time to market and handle the increasing complexity of software for real-time systems. In this paper the basic properties of an event-triggered component model for real-time software are introduced. For the early exposure of design errors a process for the simulation based validation of component-based software applying use cases is presented. A template for structuring use cases helps gathering the course-oriented requirements which describe the required behaviour of the composed software. Requirements sequence diagrams are extracted from the use cases and compared with the simulated behaviour of the component-based software. A case study of a power window control from the automotive body electronics domain demonstrates practical experience with applying use cases for the requirements validation.

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Citation: Wolfgang Fleisch, "Applying Use Cases for the Requirements Validation of Component-Based Real-Time Software," *isorc*, p. 75, Second IEEE International Symposium on Object-Oriented Real-Time Distributed Computing, 1999.

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Using Software Architecture for Code Testing

Henry Muccini
Antonia Bertolino
Paola Inverardi

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Abstract

Our research deals with the use of Software Architecture (SA) as a reference model for testing the conformance of an implemented system with respect to its architectural specification. We exploit the specification of SA dynamics to identify useful schemes of interactions between system components and to select test classes corresponding to relevant architectural behaviors. The SA dynamics is modeled by Labeled Transition Systems (LTSs). The approach consists of deriving suitable LTS abstractions called ALTSs. ALTSs offer specific views of SA dynamics by concentrating on relevant features and abstracting away from uninteresting ones. Intuitively, deriving an adequate set of test classes entails deriving a set of paths that appropriately cover the ALTS. Next, a relation between these abstract SA tests and more concrete, executable tests needs to be established so that the architectural tests derived can be refined into code-level tests. In